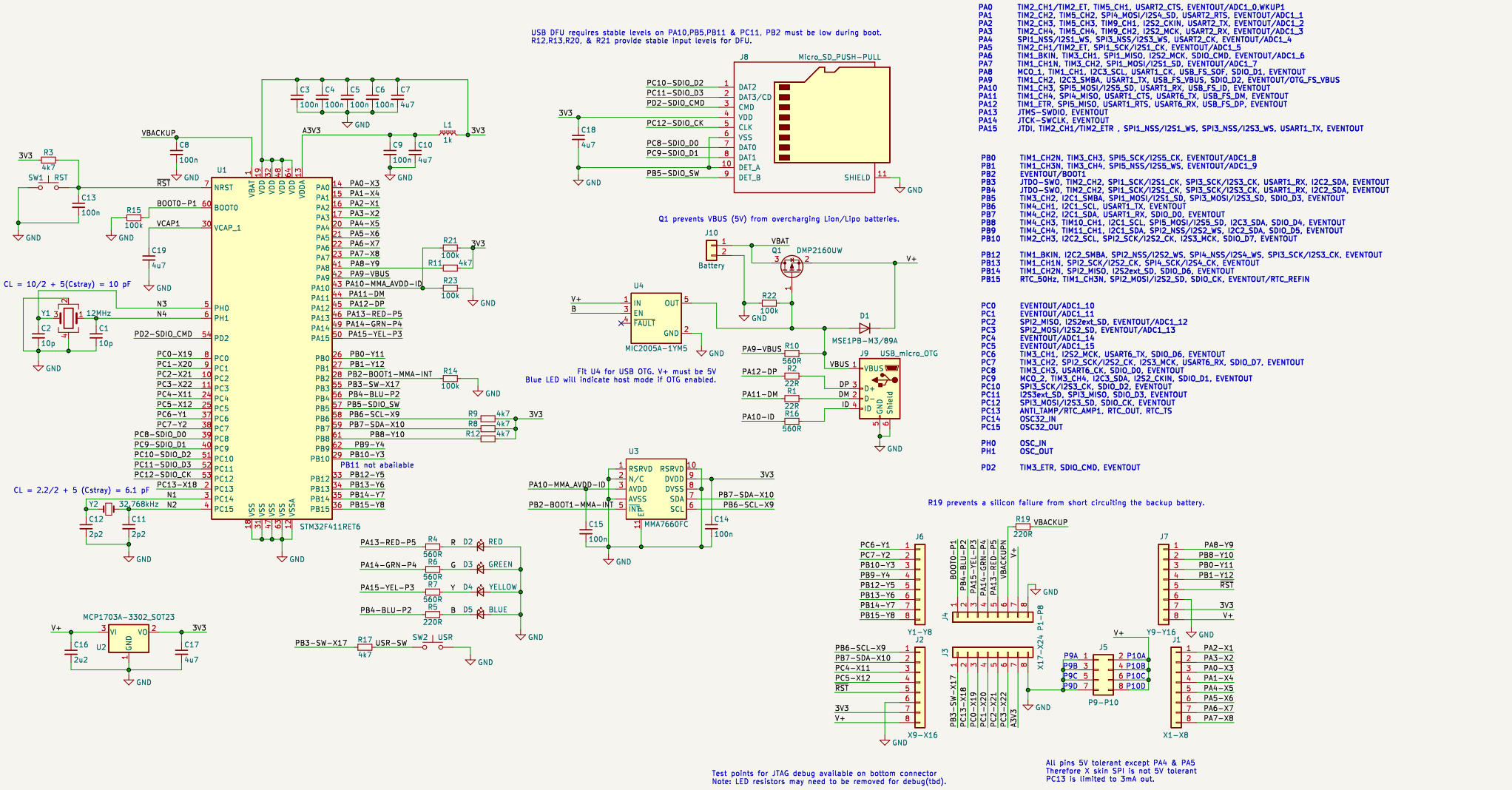
USB DFU requires stable levels on PA10,PB5,PB11 & PC11, PB2 must be low during boot.
R12,R13,R20, & R21 provide stable input levels for DFU.
PA0 TIM2_CH1/TIM2_ET, TIM5_CH1, USART2_CTS, EVENTOUT/ADC1_0,WKUP1
PA1 TIM2_CH2, TIM5_CH2, SPI4_MOSI/I2S4_SD, USART2_RTS, EVENTOUT/ADC1_1
PA2 TIM2_CH3, TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, EVENTOUT/ADC1_2
PA3 TIM2_CH4, TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, EVENTOUT/ADC1_3
PA4 SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT/ADC1_4
PA5 TIM2_CH1/TIM2_ET, SPI1_SCK/I2S1_CK, EVENTOUT/ADC1_5
PA6 TIM1_BKIN, TIM3_CH1, SPI1_MISO, I2S2_MCK, SDIO_CMD, EVENTOUT/ADC1_6
PA7 TIM1_CH1N, TIM3_CH2, SPI1_MOSI/I2S1_SD, EVENTOUT/ADC1_7
PA8 MCO_1, TIM1_CH1, I2C3_SCL, USART1_CK, USB_FS_SOF, SDIO_D1, EVENTOUT
PA9 TIM1_CH2, I2C3_SMBA, USART1_TX, USB_FS_VBUS, SDIO_D2, EVENTOUT/OTG_FS_VBUS
PA10 TIM1_CH3, SPI5_MOSI/I2S5_SD, USART1_RX, USB_FS_ID, EVENTOUT
PA11 TIM1_CH4, SPI4_MISO, USART1_CTS, USART6_TX, USB_FS_DM, EVENTOUT
PA12 TIM1_ETR, SPI5_MISO, USART1_RTS, USART6_RX, USB_FS_DP, EVENTOUT
PA13 JTMS-SWDIO, EVENTOUT
PA14 JTCK-SWCLK, EVENTOUT
PA15 JTDI, TIM2_CH1/TIM2_ETR , SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART1_TX, EVENTOUT
PB0 TIM1_CH2N, TIM3_CH3, SPI5_SCK/I2S5_CK, EVENTOUT/ADC1_8
PB1 TIM1_CH3N, TIM3_CH4, SPI5_NSS/I2S5_WS, EVENTOUT/ADC1_9
PB2 EVENTOUT/BOOT1
PB3 JTDO-SWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, I2C2_SDA, EVENTOUT
PB4 JTDO-SWO, TIM2_CH2, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, USART1_RX, I2C2_SDA, EVENTOUT
PB5 TIM3_CH2, I2C1_SMBA, SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, SDIO_D3, EVENTOUT
PB6 TIM4_CH1, I2C1_SCL, USART1_TX, EVENTOUT
PB7 TIM4_CH2, I2C1_SDA, USART1_RX, SDIO_D0, EVENTOUT
PB8 TIM4_CH3, TIM10_CH1, I2C1_SCL, SPI5_MOSI/I2S5_SD, I2C3_SDA, SDIO_D4, EVENTOUT
PB9 TIM4_CH4, TIM11_CH1, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C2_SDA, SDIO_D5, EVENTOUT
PB10 TIM2_CH3, I2C2_SCL, SPI2_SCK/I2S2_CK, I2S3_MCK, SDIO_D7, EVENTOUT
PB12 TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, SPI4_NSS/I2S4_WS, SPI3_SCK/I2S3_CK, EVENTOUT
PB13 TIM1_CH1N, SPI2_SCK/I2S2_CK, SPI4_SCK/I2S4_CK, EVENTOUT
PB14 TIM1_CH2N, SPI2_MISO, I2S2ext_SD, SDIO_D6, EVENTOUT
PB15 RTC_50Hz, TIM1_CH3N, SPI2_MOSI/I2S2_SD, SDIO_CK, EVENTOUT/RTC_REFIN
PC0 EVENTOUT/ADC1_10
PC1 EVENTOUT/ADC1_11
PC2 SPI2_MISO, I2S2ext_SD, EVENTOUT/ADC1_12
PC3 SPI2_MOSI/I2S2_SD, EVENTOUT/ADC1_13
PC4 EVENTOUT/ADC1_14
PC5 EVENTOUT/ADC1_15
PC6 TIM3_CH1, I2S2_MCK, USART6_TX, SDIO_D6, EVENTOUT
PC7 TIM3_CH2, SPI2_SCK/I2S2_CK, I2S3_MCK, USART6_RX, SDIO_D7, EVENTOUT
PC8 TIM3_CH3, USART6_CK, SDIO_D0, EVENTOUT
PC9 MCO_2, TIM3_CH4, I2C3_SDA, I2S2_CKIN, SDIO_D1, EVENTOUT
PC10 SPI3_SCK/I2S3_CK, SDIO_D2, EVENTOUT
PC11 I2S3ext_SD, SPI3_MISO, SDIO_D3, EVENTOUT
PC12 SPI3_MOSI/I2S3_SD, SDIO_CK, EVENTOUT
PC13 ANTI_TAMP/RTC_AMP1, RTC_OUT, RTC_TS
PC14 OSC32_IN
PC15 OSC32_OUT
PH0 OSC_IN
PH1 OSC_OUT
PD2 TIM3_ETR, SDIO_CMD, EVENTOUT
Q1 prevents VBUS (5V) from overcharging Lion/Lipo batteries.
Fit U4 for USB OTG. V+ must be 5V
Blue LED will indicate host mode if OTG enabled.
R19 prevents a silicon failure from short circuiting the backup battery.
CL = 10/2 + 5(Cstray) = 10 pF
CL = 2.2/2 + 5 (Cstray) = 6.1 pF
PB11 not abaliable
Test points for JTAG debug available on bottom connector
Note: LED resistors may need to be removed for debug(tbd).
All pins 5V tolerant except PA4 & PA5
Therefore X skin SPI is not 5V tolerant
PC13 is limited to 3mA out.
STM32F411RET6
MIC2005A-1YM5
MMA7660FC
MCP1703A-3302_SOT23
DMP2160UW
MSE1PB-M3/89A
Micro_SD_PUSH-PULL
USB_micro_OTG
P9-P10
X1-X8
X9-X16
Y1-Y8
Y9-Y16
P1-P8
X17-X24